WHAT IS CLAIMED IS:

1. A tape ball grid array package, comprising:

a tape having:

a dielectric layer having a first side, a second side and a plurality of via holes that pass through the dielectric layer;

a patterned first metallic layer over the first side of the dielectric layer such that one end of the via holes is closed to form a plurality of blind holes;

a patterned second metallic layer over the second side of the dielectric layer exposing the open end of the blind holes;

a patterned first solder mask layer over the first metallic layer exposing a portion of the first metallic layer to serve as a plurality of contact points;

a patterned second solder mask layer over the second metallic layer exposing a portion of the second metallic layer and the open end of the blind holes;

a plurality of solder balls inserted into the blind holes with one end of the solder balls protruding out from the surface of the second solder mask layer, wherein the solder balls and the first metallic layer are electrically connected while at least one solder ball and the second metallic layer are electrically connected; and

at leastone chip over the first side of the tape, wherein the chip connects electrically with various contact points on the tape.

2. The package of claim 1, wherein material constituting the dielectric layer includes polyimide.

3. The package of claim 1, wherein the second metallic layer serves as a power source layer or a ground layer.

4. The package of claim 1, wherein the first metallic layer serves as a signal transmission layer.

5. The package of claim 1, wherein material constituting the first metallic layer and the second metallic layer includes copper.

6. The package of claim 1, wherein the upper surface and the lower surface of the first metallic layer as well as the upper surface of the second metallic layer further include metallic alloy layers.

7. The package of claim 6, wherein material constituting the metallic alloy layer includes nickel-gold or lead-tin alloy.

8. The package of claim 1, wherein the chip has an active surface and a back surface, and the active surface of the chip further includes a plurality of bonding pads.

9. The package of claim 8, wherein the package further includes a plurality of conductive wires and packaging material, wherein the backside of the chip is attached to the first solder mask layer, the conductive wires connect the bonding pads with corresponding contact points on the tape, and the packaging material encloses the chip, the conductive wires and the contact points.

10. The package of claim 9, wherein the package further includes a stiffener on the first solder mask layer surrounding the packaging material.

11. The package of claim 8, wherein the chip further includes a plurality of bumps protruding from the bonding pads, and the bumps correspond in position to various contact points.

12. The package of claim 11, wherein the package further includes underfilling material that encloses the bonding pads, the bumps and the contact points.

13. The package of claim 11, wherein the package further includes a stiffener on the first solder mask layer and surrounds the chip.

14. A method of forming a tape ball grid array package, comprising the steps of:

providing a tape having a dielectric layer, a first metallic layer and a second metallic layer, wherein the dielectric layer has a first side and a second side, the first metallic layer is formed on the first side of the dielectric layer, and the second metallic layer is formed on the second side of the dielectric layer;

patterning the first metallic layer and the second metallic layer;

forming a plurality of blind holes in the tape, wherein the blind holes pass through the second metallic layer and the dielectric layer but stop at the first metallic layer;

forming a patterned first solder mask layer over the first metallic layer and a patterned second solder mask layer over the second metallic layer, wherein the first solder mask layer exposes a portion of the first metallic layer to form a plurality of contact points, and the second solder mask layer exposes a portion of the second metallic layer and the open end of the blind holes;

inserting a solder ball into each blind hole, wherein one end of the solder ball protrudes out the surface of the second solder mask layer and connects electrically with the first metallic layer, and at least one solder ball connects electrically with the second metallic layer; and

attaching at least one chip on the first side of the tape and connecting the chip electrically to various contact points on the tape.

15. The method of claim 14, wherein material constituting the dielectric layer includes polyimide.

16. The method of claim 14, wherein material constituting the first metallic layer and the second metallic layer includes copper.

17. The method of claim 14, wherein the second metallic layer serves as a power source layer or a ground layer.

18. The method of claim 17, wherein the first metallic layer serves as a signal transmission layer.

19. The method of claim 14, wherein the step of patterning the first metallic layer and the second metallic layer includes photolithographic and etching processes.

20. The method of claim 14, wherein after the step of patterning the first metallic layer and the second metallic layer, further includes forming a metallic alloy layer on the upper and lower surface of the first metallic layer and the upper surface of the second metallic layer.

21. The method of claim 20, wherein the step of forming the metallic alloy layer includes electroplating.

22. The method of claim 20, wherein the step of forming the metallic alloy layer includes chemical plating.

23. The method of claim 20, wherein the step of forming the metallic alloy layer includes electroless plating.

24. The method of claim 20, wherein material constituting the metallic alloy layer includes nickel-gold or tin-lead alloy.

25. The method of claim 14, wherein the step of forming a plurality of blind holes in the tape includes photolithographic and etching, laser burning or plasma etching.

26. The method of claim 14, wherein the step of forming the first patterned solder mask layer and the second patterned solder mask layer includes coating a first solder mask layer and a second solder mask layer over the first metallic layer and the second metallic layer respectively, and then photo-expose and develop the first solder mask layer and the second solder mask layer.

27. The method of claim 14, wherein the chip and the first metallic layer are electrically connected in a wire bonding operation.

28. The method of claim 14, wherein the chip and the first metallic layer are electrically connected during the fabrication of a flip-chip package.